The following Listing of Claims will replace all prior versions, and listings, of claims in the present application:

Listing of Claims:

1-20 (Canceled)

21. (Previously Presented) A multi-layer dielectric layer over a substrate for use in dual-damascene applications, comprising:

a barrier layer disposed over the substrate;

an inorganic dielectric layer disposed over the barrier layer, the inorganic dielectric layer having a dielectric constant of about 4; and

a low dielectric constant layer disposed directly over and in direct contact with the inorganic dielectric layer;

wherein the low dielectric constant layer is configured to receive metallization line trenches to define a metallization line layer and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

22. (Original) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 21, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

23. (Original) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 22, wherein the inorganic dielectric layer is one of an un-doped TEOS oxide and a fluorine doped oxide.

24. (Original) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 23, wherein the low dielectric constant layer is a carbon doped oxide.

25. (Canceled)

26. (Previously Presented) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 24, wherein the inorganic dielectric layer has different material properties than the low dielectric constant layer.

27. (Previously Presented) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 26, wherein a thickness of the inorganic dielectric layer is about 4500 Angstroms.

28. (Previously Presented) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 27, wherein a thickness of the low dielectric constant layer is about 5000 Angstroms.

29. (Previously Presented) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 26, wherein a thickness of the low dielectric constant layer is greater than a thickness of the inorganic dielectric layer.

30. (Previously Presented) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 29, wherein the thickness of the inorganic dielectric layer is about at least 1,000 Angstroms, and the thickness of the low dielectric constant layer and the inorganic dielectric layer is about 10,000 Angstroms.

31. (Previously Presented) A multi-layer inter-metal dielectric semiconductor structure, comprising:

a barrier layer disposed over a base dielectric layer;

an inorganic dielectric layer of an un-doped TEOS oxide disposed over the barrier layer;

a low dielectric constant layer of a carbon doped oxide disposed directly over and in direct contact with the inorganic dielectric layer;

wherein the low dielectric constant layer is configured to receive metallization line trenches to define a metallization line layer and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

32. (Previously Presented) A multi-layer inter-metal dielectric semiconductor structure as recited in claim 31, wherein a thickness of the inorganic dielectric layer of an un-doped TEOS oxide is about 4500 Angstroms.

33. (Previously Presented) A multi-layer inter-metal dielectric semiconductor structure as recited in claim 32, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is about 5000 Angstroms.

34. (Previously Presented) A multi-layer inter-metal dielectric semiconductor structure as recited in claim 31, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is greater than a thickness of the inorganic dielectric layer of an un-doped TEOS oxide.

35. (Previously Presented) A multi-layer inter-metal dielectric semiconductor structure as recited in claim 34, wherein the thickness of the inorganic dielectric layer of an un-doped TEOS oxide is about at least 1,000 Angstroms, and the thickness of the low dielectric constant layer of a carbon doped oxide and the inorganic dielectric layer of an un-doped TEOS oxide is about 10,000 Angstroms.

36. (Previously Presented) A dielectric structure for dual-damascene applications, comprising:

a barrier disposed over a base dielectric;

an inorganic dielectric layer of a fluorine doped oxide disposed over the barrier;

a low dielectric constant layer of a carbon doped oxide disposed directly over and in direct contact with the inorganic dielectric layer;

wherein the low dielectric constant layer is configured to receive metallization line trenches to define a metallization line layer and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

37. (Previously Presented) A dielectric structure for dual-damascene applications as recited in claim 36, wherein a thickness of the inorganic dielectric layer of a fluorine doped oxide is about 4500 Angstroms.

38. (Previously Presented) A dielectric structure for dual-damascene applications as recited in claim 37, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is about 5000 Angstroms.

39. (Previously Presented) A dielectric structure for dual-damascene applications as recited in claim 36, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is greater than a thickness of the inorganic dielectric layer of a fluorine doped oxide.

40. (Previously Presented) A dielectric structure for dual-damascene applications as recited in claim 39, wherein the thickness of the inorganic dielectric layer of a fluorine doped oxide is about at least 1,000 Angstroms, and the thickness of the low dielectric constant layer of a carbon doped oxide and the inorganic dielectric layer of a fluorine doped oxide is about 10,000 Angstroms.

41. (Previously Presented) A multi-layer dielectric disposed over a substrate for use in dual-damascene applications, comprising:

a barrier layer disposed over the substrate;

an inorganic dielectric layer of a fluorine doped oxide disposed over the barrier layer, the inorganic dielectric layer having a first thickness; and

a low dielectric constant layer of a carbon doped oxide disposed directly over and in direct contact with the inorganic dielectric layer, the low dielectric constant layer having a second thickness and defining a metallization line layer;

wherein metallization lines are formed in a first portion of the second thickness of the low dielectric constant layer, and a via path is configured to be defined in an entire portion of the first thickness of the inorganic dielectric layer and in at least a portion of the second thickness of the low dielectric constant layer.

42. (New) The multi-layer dielectric of claim 41, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

43. (New) The multi-layer dielectric of claim 41, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is greater than a thickness of the inorganic dielectric layer of a fluorine doped oxide.

44. (New) The multi-layer dielectric of claim 41, wherein the inorganic dielectric layer has different material properties than the low dielectric constant layer.

45. (New) The multi-layer dielectric of claim 41, wherein a thickness of the inorganic dielectric layer is about 10,000 Angstroms.

46. (New) The multi-layer dielectric of claim 41, wherein a thickness of the low dielectric constant layer is about 10,000 Angstroms.

47. (New) A multi-layer dielectric disposed over a substrate, comprising:

a barrier layer disposed over the substrate;

an inorganic dielectric layer disposed over the barrier layer, the inorganic dielectric layer having a first thickness; and

a low dielectric constant layer disposed over the inorganic dielectric layer, the low dielectric constant layer having a second thickness and defining a metallization line layer;

wherein metallization lines are formed in a first portion of the second thickness of the low dielectric constant layer, and a via path is configured to be defined in an entire portion of the first thickness of the inorganic dielectric layer and in at least a portion of the second thickness of the low dielectric constant layer.

48. (New) The multi-layer dielectric of claim 47, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

49. (New) The multi-layer dielectric of claim 47, wherein the inorganic dielectric layer is one of an un-doped TEOS oxide and a fluorine doped oxide.

50. (New) The multi-layer dielectric of claim 47, wherein the low dielectric constant layer is a carbon doped oxide.

51. (New) The multi-layer dielectric of claim 47, wherein the inorganic dielectric layer has different material properties than the low dielectric constant layer.

52. (New) The multi-layer dielectric of claim 47, wherein a thickness of the inorganic dielectric layer is about 10,000 Angstroms.

53. (New) The multi-layer dielectric of claim 47, wherein a thickness of the low dielectric constant layer is about 10,000 Angstroms.

54. (New) The multi-layer dielectric of claim 47, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is greater than a thickness of the inorganic dielectric layer of a fluorine doped oxide.